

**P-Channel Enhancement-Mode MOS Transistors****Product Summary**

Part Number	$V_{(BR)DSS}$ Min (V)	$V_{GS(th)}$ (V)	$r_{DS(on)}$ Max ( $\Omega$ )	$I_{D(on)}$ Min (mA)	$C_{rss}$ Max (pF)	$t_{ON}$ Typ (ns)
3N163	-40	-2 to -5	250	-5	0.7	18
3N164	-30	-2 to -5	300	-3	0.7	18

**Features**

- Ultra-Low Input Leakage: 0.02 pA Typ.
- High Gate Breakdown Voltage:  $\pm 125$  V
- Normally Off

**Benefits**

- High Input Impedance Isolation
- Minimize Handling ESD Problems
- High Off Isolation without Power

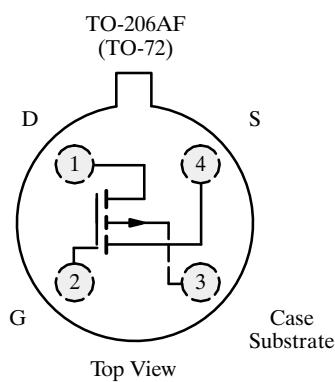
**Applications**

- Ultra-High Input Impedance Amplifier
- Smoke Detectors
- Electrometers
- Analog Switching
- Digital Switching

**Description**

The 3N163/164 are lateral p-channel MOSFETs designed for analog switch and preamplifier applications where high speed and low parasitic capacitances are required.

The hermetic TO-206AF package is compatible with military processing per military standards (see Military information).

**Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

Drain-Source Voltage (3N163) .....	-40 V	Storage Temperature .....	-65 to 200°C
(3N164) .....	-30 V	Operating Junction Temperature .....	-55 to 150°C
Gate-Source Voltage .....	$\pm 30$ V	Power Dissipation <sup>a</sup> .....	375 mW
Continuous Drain Current .....	-50 mA		
Lead Temperature (1/16" from case for 10 seconds) .....	300°C	Notes:	
		a.	Derate 3 mW/°C above 25°C

# 3N163/164

TEMIC

Siliconix

## Specifications<sup>a</sup>

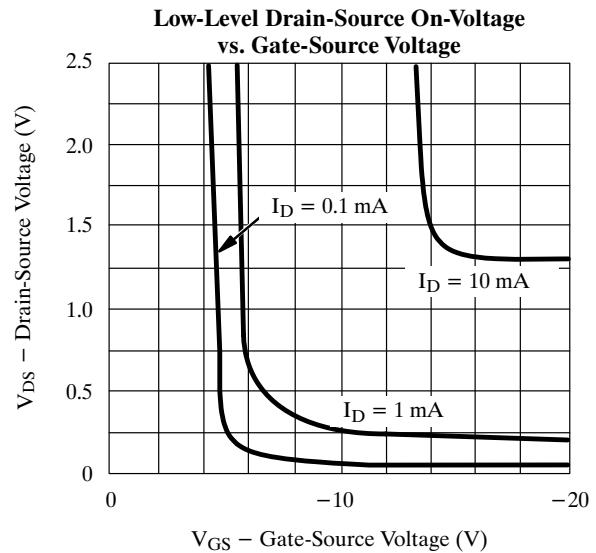
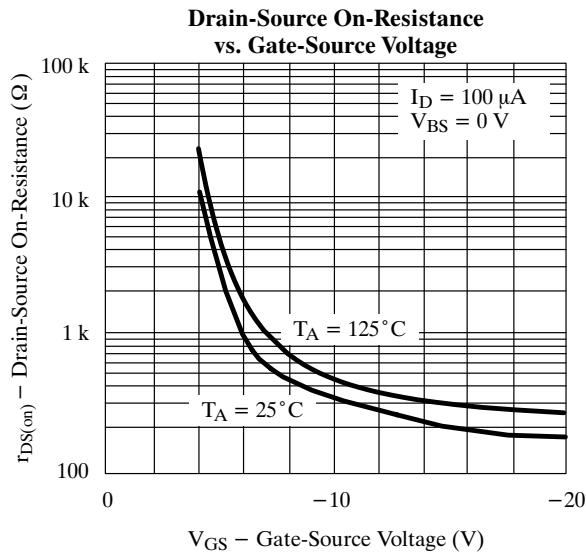
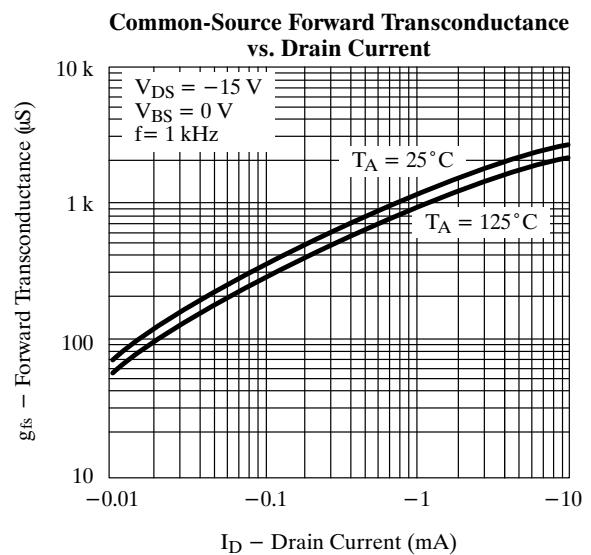
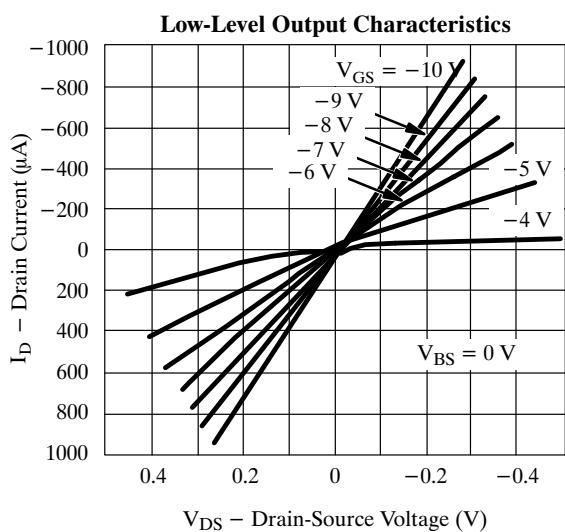
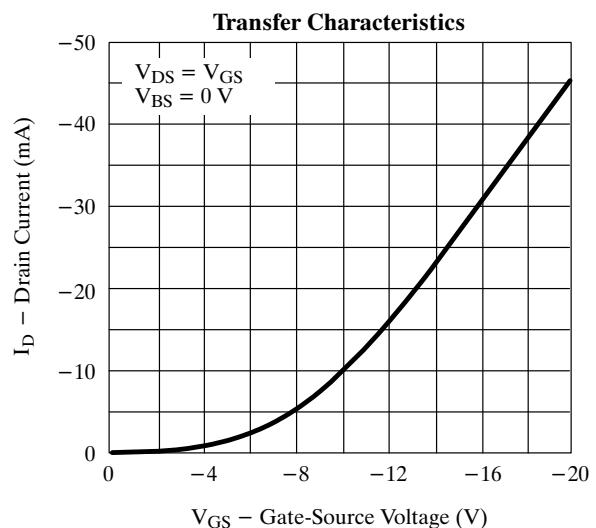
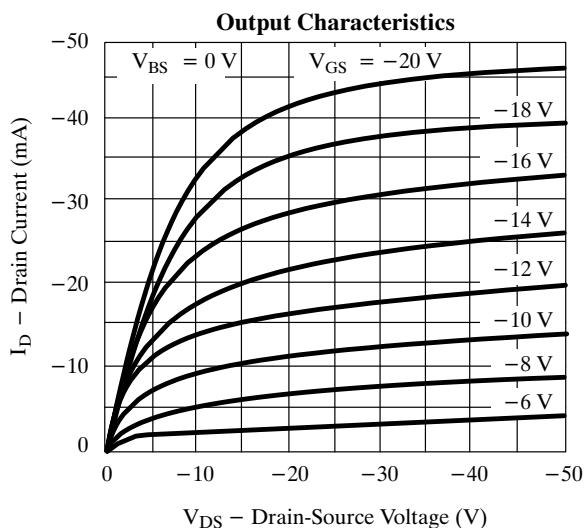
Parameter	Symbol	Test Conditions	Typ <sup>b</sup>	Limits				Unit	
				3N163		3N164			
				Min	Max	Min	Max		
<b>Static</b>									
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = -10 µA, V <sub>DS</sub> = 0 V	-70	-40		-30		V	
Source-Drain Breakdown Voltage	V <sub>(BR)SDS</sub>	I <sub>S</sub> = -10 µA, V <sub>GD</sub> = V <sub>BD</sub> = 0 V	-70	-40		-30			
Gate-Threshold Voltage	V <sub>GS(th)</sub>	I <sub>D</sub> = -10 µA, V <sub>GS</sub> = V <sub>DS</sub>	-2.5	-2	-5	-2	-5		
Gate-Source Voltage	V <sub>GS</sub>	I <sub>D</sub> = -0.5 mA, V <sub>DS</sub> = -15 V	-3.5	-3	-6.5	-2.5	-6.5		
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = -40 V, V <sub>DS</sub> = 0 V	<-1		-10			pA	
		T <sub>A</sub> = 125°C <sup>d</sup>	-1						
		V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	<-1				-10		
		T <sub>A</sub> = 125°C <sup>d</sup>	-1						
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V	-8		-200		-400	nA	
		T <sub>A</sub> = 125°C <sup>d</sup>	-20						
Zero-Gate Voltage Source Current	I <sub>SDS</sub>	V <sub>GD</sub> = V <sub>BD</sub> = 0 V, V <sub>SD</sub> = -20 V	-10		-400		-800	pA	
		T <sub>A</sub> = 125°C <sup>d</sup>	-25					nA	
On-State Drain Current <sup>c</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -10 V	-10	-5	-30	-3	-30	mA	
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>GS</sub> = -20 V, I <sub>D</sub> = -100 µA	180		250		300	Ω	
		T <sub>A</sub> = 125°C <sup>d</sup>	270						
<b>Dynamic</b>									
Forward Transconductance <sup>c</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 mA f = 1 kHz	2.7	2	4	1	4	mS	
Common-Source Output Conductance <sup>c</sup>	g <sub>os</sub>		150		250		250	µS	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 mA f = 1 MHz	2.4		3.5		3.5	pF	
Output Capacitance	C <sub>oss</sub>		2.5		3		3		
Reverse Transfer Capacitance	C <sub>rss</sub>		0.5		0.7		0.7		
<b>Switching</b>									
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 1500 Ω I <sub>D</sub> ≈ -10 mA, V <sub>GEN</sub> = -12 V R <sub>G</sub> = 50 Ω	5		12		12	ns	
	t <sub>r</sub>		13		24		24		
Turn-Off Time	t <sub>d(off)</sub>		25		50		50		

Notes:

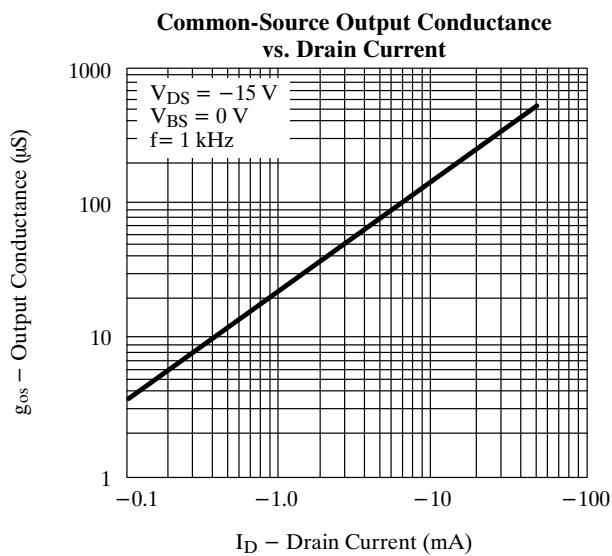
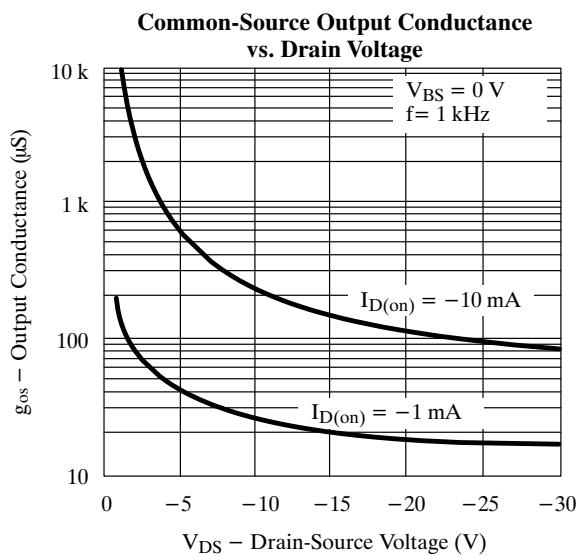
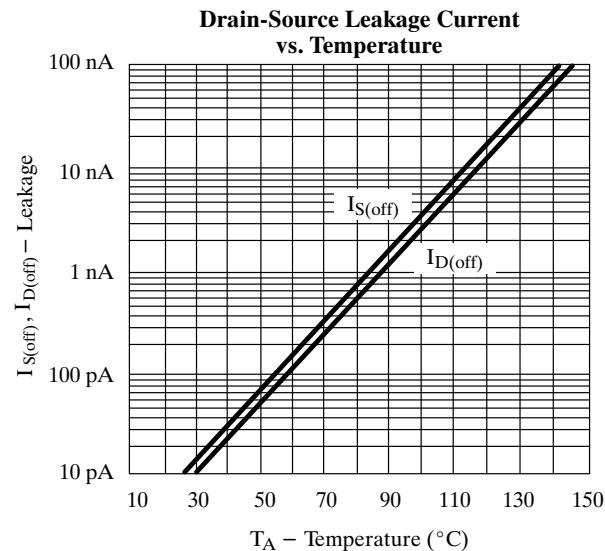
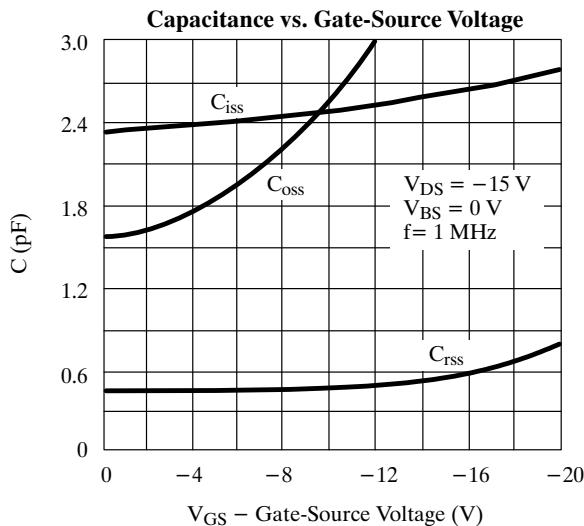
- a. T<sub>A</sub> = 25°C unless otherwise noted.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.
- d. This parameter not registered with JEDEC.
- e. Switching time is essentially independent of operating temperature.

MRA

## Typical Characteristics



### Typical Characteristics (Cont'd)



### Switching Time Test Circuit

